REMARKS

Entry of this Amendment is proper under 37 CFR §1.116, since no new issues are raised and the claim amendments reduce the number of issues for Appeal by addressing the rejection under 35 USC §112, second paragraph, and attempting to clarify the current confusion over claim terminology.

Claims 1, 3, 5-7, 9, and 11-20 are all the claims presently pending in the application. Claims 2, 4, 8, and 10 are canceled as being redundant to the changes made to independent claims 1 and 7. New claim 20 attempts to add additional clarification to the wording change of independent claim 1, should the Examiner consider that additional clarification is desirable.

The Examiner objects to claims 1-6, 9-12, and 19 because of the "and/or" terminology. Although Applicants believe that this terminology is completely acceptable since it is readily understood by one having ordinary skill in the art, they have amended the claims in a manner believed appropriate for the Examiner's concerns. Accordingly, Applicants request that the Examiner reconsider and withdraw this objection.

It is noted that Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 2, 4, 8, 10, 14, and 17 stand rejected under 35 USC §112 as allegedly being incomplete for omitting essential structural cooperative relationships of elements as caused by the use of the term "discriminating." As explained below, the present invention modifies conventional power consumption calculations for storage elements by using the clock-based simulation method for its speed (relative to much slower gate-level simulations such as RTL HDL) as modified to be able to track each bit in the storage element. The type of storage element (e.g., register versus memory) is determined (e.g., "discriminated") by using the information of the behavioral synthesis. Therefore, with this explanation, although Applicants believe that one having ordinary skill in the art would readily understand the meaning intended, particularly in view of the description in the specification, the above claim amendments have been amended to replace "discriminating" with "determining" to expedite prosecution and request that the Examiner reconsider and withdraw this rejection.

Claims 1-19 stand rejected under 35 USC §102(e) as allegedly anticipated by US Patent 6,782,354 to Ikegami.

This rejection is respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

As described and as defined in, for example, claim 1, the claimed invention is directed to an apparatus for estimating power consumption. A behavioral synthesis unit to which an algorithm-level description is input converts the algorithm-level description to a clock-based description and behavioral synthesis information. A clock-based simulation unit to which the clock-based description and behavioral synthesis information are input executes a clock-based simulation and calculates a power consumption factor of a storage element based upon both the clock-based description and behavioral synthesis information. The power consumption factor of the storage element is calculated by determining whether an array variable in the clock-based description is mapped to a memory or registers, using the behavior synthesis information for making this determination.

Conventional methods, as described beginning at line 12 on page 1, can be broken down into either an RTL HDL simulation (down to the gate level) or a clock-based simulation. As explained at lines 1-3 on page 3, the clock-based description has a lower level of abstraction than the algorithmic language and a higher level of abstraction than the RTL HDL. As stated at lines 6-8 of page 10, the RTL HDL simulation is much slower than clock-based simulation, thereby allowing the present inventors to recognize that perhaps the benefits of both basic methods can be somehow combined relative to calculating power consumption estimations.

Therefore, in contrast to the conventional method, the present invention uses the clock-based simulation because of its inherent speed. Then, as the behavioral synthesis information is available, the specific form of storage developed by the behavioral synthesis process can be determined (e.g., whether a storage unit ended up being a memory or a register or register bank), thereby allowing the power consumption factor to be precisely calculated for the resultant type of storage. Therefore, the present invention retains both the speed of the clock-based simulation and the accuracy of conventionally slower simulations.

II. THE PRIOR ART REJECTION

The Examiner alleges that Ikegami teaches the claimed invention defined by claims 1-19. Applicants respectfully disagree.

First, as pointed out by the Examiner in the Office Action, the present Application is related to Ikegami by at least the reason of a common assignee. Additionally, there are other similarities, as can be readily seen by noting that Figure 3 of the present Application is quite similar to Figure 5 of Ikegami, Figure 4 is quite similar to Figure 9, Figures 5 and 6 have similarities with Figures 6 and 7, and Figure 7 has similarities to Figure 8.

These similarities are due at least in part because both Ikegami and the present invention address a simulation tool that includes both behavior synthesis and clock-based simulation.

However, in contrast to Ikegami, the present invention addresses the specific problem of calculating power consumption of memory elements. There is no corresponding methodology used in Ikegami and the power calculations therein are sparsely described.

As explained beginning at line 6 on page 3 of the instant Application, estimating power consumption using RTL HDL involves updating all gate values for all cycles, thereby causing this power consumption calculation method to be slow. In contrast, the present invention provides a method wherein the high speed clock-based simulation is used, during which simulation the storage elements are represented in an abstract format (e.g., an array) in which details of each bit is retained but there is no need for the time-consuming task characteristic of RTL HDL simulations to check all gates during each cycle. Therefore, using the clock-based simulation allows the power consumption calculations to proceed at a much higher speed relative to RTL HDL simulation.

One of the techniques used in the present invention is that, as the behavioral synthesis proceeds, the type of the storage elements can be determined, thereby allowing the power consumption calculations to be further refined, based upon knowing whether each storage element has the power consumption characteristics that are specific to, for example, a register, memory block, etc.

In contrast, at line 26 of column 9, Ikegami specifically refers to the RTL HDL model as used for the power consumption estimation. This reference seems to be the only power

consumption discussion in Ikegami and is clearly different from the claimed invention. Therefore, even if there are other similarities between Ikegami and the present invention, the present invention uses a method for power consumption calculation that clearly differs from the RTL HDL-based method that is described in Ikegami.

Hence, turning to the clear language of the claims, in Ikegami there is no teaching or suggestion of: "... calculating a power consumption factor of a storage element, based upon both the clock-based description and behavioral synthesis information, wherein the power consumption factor of the storage element is calculated by determining whether an array variable in the clock-based description is mapped to a memory or registers, using the behavioral synthesis information."

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Ikegami. Therefore, the Examiner is respectfully requested to reconsider and withdraw this rejection based on Ikegami.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1, 3, 5-7, 9, and 11-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 4/13/06

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CERTIFICATION OF TRANSMISSION

I certify that I transmitted via facsimile to (571) 273-8300/-1905 this Amendment under 37 CFR §1.116 to Examiner Y. Rossoshek on April 13, 2006.

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